Unit 3 : Sequential Circuit

Lesson 1 : Sequential Logic Circuit

1.1. Learning Objectives

On completion of this lesson you will be able to :

- define sequential circuit
- know the different types of sequential circuit
- understand clock and its classification
- know about flip-flop and latches.

1.2. Sequential Circuits

In sequential logic circuit, "the present values of outputs are dependent on both present values of the inputs and the past values of inputs.

We already know that the combinational circuits implements the essential functions of a digital computer. *"A circuit known as combinational as long as its steady state outputs depend only on its current inputs".* In these circuits, there is no ability to retain the information regarding the state of the circuit and any prior input level conditions have no effect on the present outputs because they provide no memory. So for the later purposes, sequential circuit is used. *In sequential logic circuit, the present values of outputs are dependent on both present values of the inputs and the past values of inputs.* A sequential logic circuit consist of two parts.

- *the memory elements* i.e. flip-flop which is made up of an assembly of logic gates.
- *the combinational logic circuits* needed to produce the excitation inputs to the memory elements and to produce the required outputs.

Sequential circuits find wide application in digital systems as counters, registers, control logic, memories and other complex functions.

Examples,

- The elevator control.
- The traffic light system.
- automatic lock - which remember the combination of numbers and also their sequence.

Basic Block

A general model of a sequential circuit is shown in the following Fig.3.1.

Output depends on present state and input.

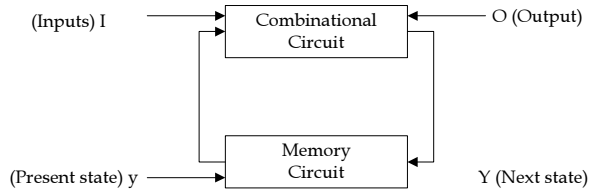


Fig. 3.1 : Block diagram of sequential circuit logic.

So, from the block diagram, we can find.

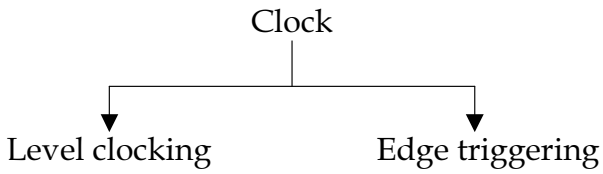
Output depends on present state and input i.e.

output O = f (I, y)
next state Y = f (I, y)
present state y = f (Y)

1.3. Clock

Clock is periodic sequence of pulses. Clock can be classified as level clocking and edge triggering.

Clock is periodic sequence of pulses.



Purposes

The purposes of clock is to synchronize the over-all action and to prevent the flip-flop from changing states until the right time.

a) ***Level clocking :*** The Flip-flop responds to the level (high or low) of the clock signal. Level clocking is of two types.

i) positive clocking

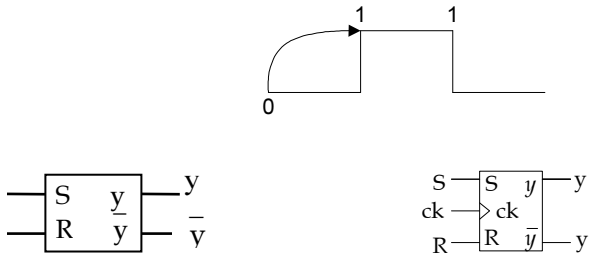


Fig. 3.2(a) : Basic block of latch (SR).

ii) negative clocking

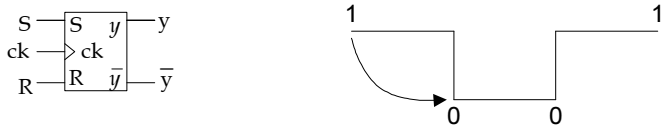


Fig. 3.2 (b) : negative clocking.

b) ***Edge Triggering :*** The flip-flop responds only on the rising or falling edge of the clock. Edge triggering is of two types. These are as follows :

The flip-flop responds only on the rising or falling edge of the clock.

i) positive edge triggering

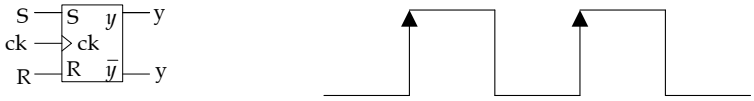


Fig. 3.3 (a) : positive edge triggering.

ii) negative edge or falling (trailing edge)

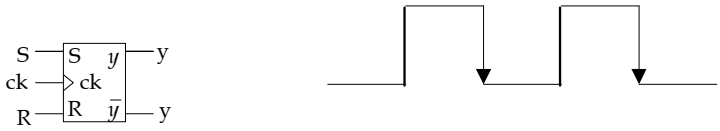


Fig. 3.3 (b) : negative edge triggering.

1.4. Types of Sequential Logic Circuits

Depending upon the timing of sequential circuit signal, the sequential logic circuits can be divided into two classes.

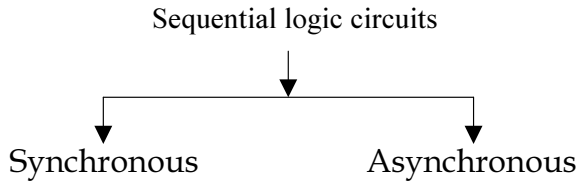


Fig. 3.4: Classes of sequential logic circuits.

Synchronous Sequential Circuits

A synchronous sequential circuits is one in which the contents of the memory can change only at discrete instants time or on the of transitions of a clock.

A synchronous sequential circuits is one in which the contents of the memory can change only at discrete instants time or on the of transitions of a clock. Since all the circuit action will take place under the control of a clock, so these circuits are known as clocked sequential circuit.

Advantage

They are easier to troubleshoot and design because its outputs can change only at specific instants of time i.e. every thing is synchronized to the clock signal transition.

Asynchronous Sequential Logic Circuits

An asynchronous sequential logic circuits is one whose outputs can change state at any instant of time with the change of one or more of the inputs.

An asynchronous sequential logic circuits is one whose outputs can change state at any instant of time with the change of one or more of the inputs. The memory elements used in these systems are delay type memory elements. It can be regarded as combinational circuit with feed back.

Disadvantage

It is difficult to design and troubleshoot and used only for simple configuration.

1.5. Flip-flops (FF)

A FF is an electronic device that has two stable states. One state is assigned the logic 1 value and the other is the logic 0. In other words, the memory elements used in sequential circuits are the flip flop. These circuits are binary cells capable of storing one bit of information.

Latch

A latch is a bistable circuit that is the fundamental building block of a flip-flop.

A latch is a bistable circuit that is the fundamental building block of a flip-flop. It exists in one of the two states (e.g. 1 and 0), and in the absence of the input, it remains in that state. It has two output y and $\bar{y}$.

The following Fig. 3.5 illustrate a simple FF or 1 bit memory (i.e. it can store one bit of information y = 0 or y = 1) and since this information is locked or latched so, this FF is known as a latch.

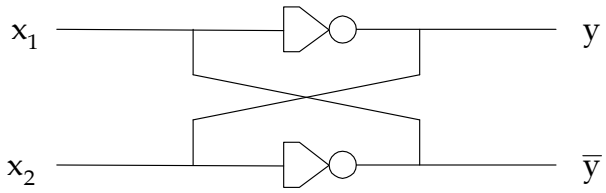


Fig. 3.5 : Simple FF or latch.

1.6. Exercise

1.6.1. Multiple choice questions

a) In sequential logic circuit the present values of outputs are dependent on

i) past values of input
ii) present values of input
iii) both present values of the inputs and the past values of inputs
iv) none of them.

b) The purpose of clock is to

i) synchronize the overall action and to prevent the FF from changing state until the right time
ii) synchronize the overall action
iii) respond the clock signal
iv) none of the above.

c) In synchronous sequential logic circuit, contents of the memory can change

i) only at discrete instants of time
ii) at any instant of time
iii) continuously
iv) none of the above.

1.6.2. Questions of short answers

a) What do you mean by sequential logic circuit and combinatioal logic circuits?
b) What do you mean by latch and FF?
c) What are the main differences between synchronous and asynchronous sequential logic circuit?

d) List some of the advantages of synchronous sequential logic circuit and disadvantages of asynchronous sequential logic circuit?
e) Distinguish between combinational and sequential Logic Circuit?

1.6.3. Analytical questions

a) i) What is clock? Describe different types of clock? ii) What is the purpose of clock signal?
b) How many types of sequential logic circuits? Describe briefly.

Lesson 2 : SR (Set - Reset) Flip-Flop

2.1. Learning Objectives

On completion of this lesson, you will be able to :

- understand the design and working principle of S-R flip-flop
- understand the design and working principle of clocked S-R flip-flop.

2.2. S-R FF

S-R flip-flop. The circuit as two input Set (S) and Reset (R) and two outputs.

The following Fig. 3.6(a) is known as S-R flip-flop. The circuit as two input Set (S) and Reset (R) and two outputs. As the starting point, assume that S=0, R=0 and y=0. The input to the gate 2 are R=0, $\bar{y}$=0, so output y = 1. The inputs to gate1 are S=0, $\bar{y}$=1, which has the output $\bar{y}$= 0. Now the state of the circuit is internally consistent and remains stable as long as S=R=0.

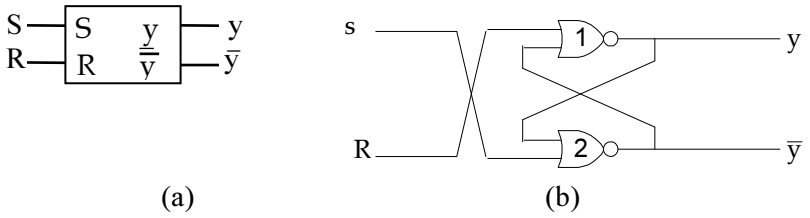


Fig. 3.6(a) : Symbol of S-R FF. Fig. 3.6(b) : S-R FF using NOR gate.

At time t_1, if S goes to 1 i.e. inputs to the gate 2 are S=1, y=0, then after a delay of Δt_2, the output of gate 2 will $\bar{y}$=0. At this point, the input to the gate 1 become R=0, $\bar{y}$=0 and after another delay Δt_1, the output of gate 1 will be y=1. This condition is stable and FF is said to be Set. If S goes to 0, the output will remain y=1, $\bar{y}$=0 i.e. unchanged. When R goes to 1 and while S=0, it forces y=0 and $\bar{y}$=1 and the circuit is said to be Reset. So, this flip-flop is called Set (S) Reset (R) flip-flop. The input combination S=R=1 is an indeterminate condition which gives y= $\bar{y}$=0 and is not allowed. The S-R FF can be defined with a truth table called transition table for the various input combinations and denoting present state by y and next state by $\bar{y}$. (Fig. 3.6). An equation describing the relationship for the next state in terms of present inputs and present states of the FF is known as characteristics equation of the FF. The characteristics equation can be got by its K-map (Fig. 3.6(c) using transition table (Fig. 3.6(e). The equation is

$Y=S+\bar{R}\,y$

SR \ y	0	1
00	0	1
01	0	0
11	x	x
10	1	1

$Y = S + \bar{R}y$

Fig. 3.6(c) : K-map.

The SR FF Circuit using *Nand* Gate

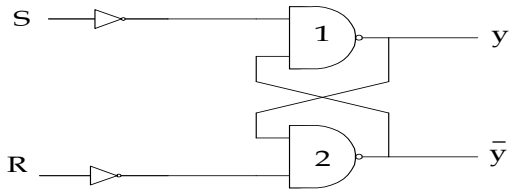


Fig. 3.6(d) : SR FF using NAND gates.

SR FF using NAND gates.

S	R	y	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

Transition Table

S	R	Y	(output)
0	0	y	(no change)
0	1	0	
1	0	1	
1	1	X	(indeterminate)

Simplified Transition Table

Fig. 3.6(e) : Transition Table for S-R FF.

2.3. Clocked S-R FF

The FFs that we have discussed before are asynchronous S-R FF, because the output changes after a brief time delay in response to a change in the input. As the events in the digital computer are synchronized to a clock pulses, so it is required to set or reset a FF in synchronism with clock pulses i.e. changes occur only when a clock pulse occurs. This is done by adding two inputs NAND gates (gate 3 and gate 4 in the Fig. 3.6(g)) with the clock pulse to the inputs of the

asynchronous S-R FF as shown in Fig 3.6(g). In order to operate these devices effectively, the following conditions must be met:

- The FF inputs should be allowed to change only when CK =0.
- The clock input should stay long enough time so that the outputs will be able to reach steady state.
- The condition S=R=1 must not be allowed to occur when CK=1.

Note : The circuit action can occur only when CK=1, when CK=0, the FF outputs do not change.

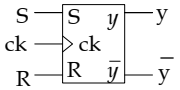


Fig. 3.6(f) : Logic symbol.

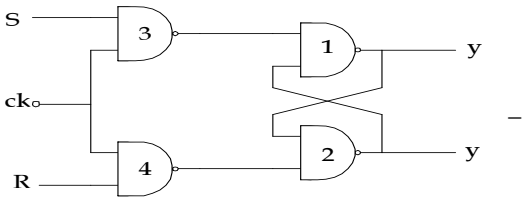


Fig. 3.6(g) : NAND gate circuit.

Logic symbol and NAND gate circuit.

Input			Output	
CK	S	R	Mode	Y
O	-	-	No action	y
∏	0	0	Hold	y
∏	0	1	Reset	0
∏	1	0	Set	1
∏	1	1	Invalid	-

Fig. 3.6(h) : Truth Table for clocked S-R FF.

2.4. Exercise

2.4.1. Multiple choice questions

a) Which one of following statement in true?

i) In synchronous S-R FF, the output changes after a brief time delay in response to a change in the input.
ii) In asynchronous S-R FF time delay in response to a change in the input.
iii) The clocked S-R FF outputs should be allowed to change only when CK = 1.
iv) none of the above.

b) Which one is the true statement?

i) When S = R = 0, output is unchanged
ii) When S = 0, R = 1, then output is 1
iii) When S = 1, R = 1, then output is 1
iv) When S = 1, R = 0, then output is indeterminate condition.

2.4.2. Questions of short answers

a) Why is the S-R FF called Set-Reset FF? Deduce the transition table for the S-R FF.
b) What do you mean by characteristic equation? Write K-map of S-R FF and characteristics equation.
c) What are the conditions that must be met in clocked S-R FF?
d) Deduce the restrictions which must be imposed upon the inputs S and R for correct operation of the bistable.

2.4.3. Analytical questions

a) Draw S-R FF using NAND gate, explain its operation.
b) What will be the state of y and $\bar{y}$ after FF has been cleared?
c) Draw S-R FF using NOR and explains its operation.

Lesson 3 : J-K Flip-Flop

3.1. Learning Objectives

On completion of this lesson, you will be able to :

- understand the design and working principle of J-K FF
- describe race around condition
- know how can race around condition can be avoided
- illustrate master-slave J-K FF.

3.2. J-K Flip-flop

Refined FF is known as the JK FF.

We saw that the clock SR FF has an indeterminate state when S=R=1. When using clocked SR FFs the designer is required to be cautious about the FF inputs. This troublesome restrictions S=R=1 can be removed by modifying the SR FF. This refined FF is known as the JK FF. This modifications involves feeding the outputs of the FF back into the inputs of circuit shown in Fig. 3.7(b). The J input alone performs *set* function causing the output (next state) to be 1. The K input alone performs *reset* function causing the output (next state) to be 0. When both J and K are 1, the next state of the FF is the complement of the present state i.e. output (next state) is reversed. When J=K=0, then output is unchanged. The block diagram, FF circuit, transition table and K map of JK FF are shown in the following (Fig. 3.7(a), 3.7(b), 3.7© and 3.7(d).

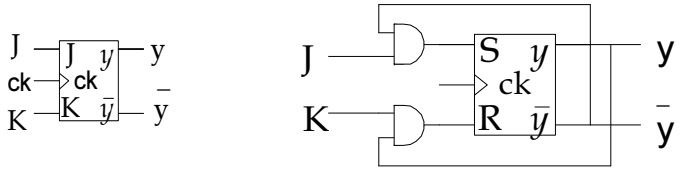


Fig. 3.7(a) : logic symbol. Fig. 3.7(b) : Modification of S-R into J-K FF.

J	K	y	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

→

J	K	Y	
0	0	y	(Hold)
0	1	0	Reset
1	0	1	Set
1	1	$\bar{y}$	Toggle (complements)

Simplified Transition Table

Fig. 3.7© : Transition Table.

JK \ Y	0	1
00	0	1
01	0	0
11	1	0
10	1	1

Fig. 3.7(d) : K - map of J-K FF.

$Y = J\bar{y} + \bar{K}y$ is the characteristic equation of JK.

3.3. Characteristic Equation of JK from Characteristic Equation of S-R FF

We know that characteristic equation of S-R FF is $Y = S + \bar{R}y$.

Substitute $S = J\bar{y}$ and $R = Ky$

$Y = J\bar{y} + \overline{Ky}.y$

$= J\bar{y} + (\bar{K} + \bar{y}).y$ (from Demorgan law $(\overline{x_2 x_1}) = \bar{x}_1 + \bar{x}_2$)

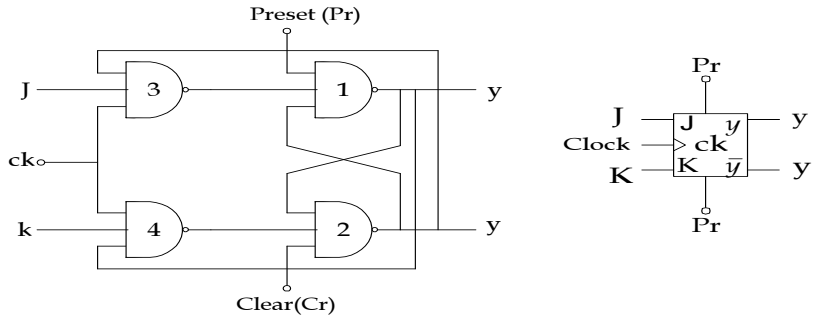
Characteristic equation of S-R FF.

$= J\bar{y} + \bar{K}y + y.y$

$= J\bar{y} + \bar{K}y + 0$ (Because $\bar{y}.y = 0$)

$\therefore Y = J\bar{y} + \bar{K}y$. This is the characteristics equation of J-K FF.

So, J-K FF can be constructed out of S-R FF and two NAND gates as shown in Fig. 3.7(e).



(e)

Fig. 3.7(e) : Logic circuit of J-K flip-flop.

The initial state of the flip-flop can be assigned by addition of two inputs namely preset and clear.

The initial state of the flip-flop can be assigned by addition of two inputs namely preset and clear as shown in Fig. 3.7(e) allows the initial state of the flip-flop to be assigned. The flip-flop can be cleared by setting $C_r=0$, $P_r=1$, $C_k=0$, as the output of gate 2 becomes 1 and the flip-flop can be preset with $P_r=0$, $C_r=1$, $C_k=0$. The FF can be enabled with $P_r=1$, $C_r=1$.

These inputs are called asynchronous inputs, and are not in synchronism with the clock and may be applied any time in between clock pulses.

3.4. Exercises

3.4.1. Multiple choice question

a) Which one of the following statement is true?

i) The K input alone performs Reset function.
ii) The K input alone performs Reset function causing the output to be 0.
iii) The J input alone performs Reset function.
iv) None of the above.

3.4.2. Question for short answers

a) Why J-K FF used?
b) What are the modification of S-R FF ? Illustrate with diagram.
c) Describe the working principle of J-K FF.
d) Draw the circuit diagram of J-K FF.
e) How can characteristic equation of J-K FF be got from that of S-R FF?

3.4.3. Analytical question

a) What is master slave J-K FF? Illustrate its operation.

Lesson 4 : D Flip Flop and T Flip Flop

4.1. Learning Objectives

On completion of this lesson, you will be able to :

- understand the design and working principle of D FF
- understand the design and working principle of T FF
- conversion of D from T and T from D.

4.2. D Flip Flop

The following Fig. 3.8(a) is the D Flip-flop.

The delay flip-flop or D flip-flop Fig. 3.8(a) which gives a unit time delay between the input and output. The input is transferred to the output at the next clock pulse. The symbol, transition table and the K-map for D-type flip-flop are shown in Fig. 3.8(a), Fig. © and Fig. (d) respectively. The next state of the D-type flip-flop is given by

The delay flip-flop or D flip-flop.

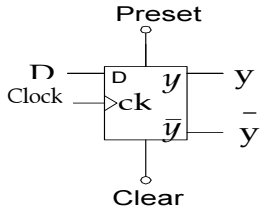


Fig. : 3.8(a) : Symbol.

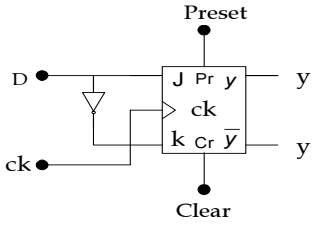


Fig. : 3.8(b) : J-K to D conversion.

D	y	Y
0	0	0
0	1	0
1	0	1
1	1	1

D	Y
0	0
1	1

Y=D

Fig. 3.8© : Transition table.

y \ d	0	1
0	0	1
1	0	1

Y=D

Fig. 3.8(d) : K-map.

D From J-K FF

A D-type flip-flop can be constructed from a J-K flip-flop by putting J = D and K = $\bar{D}$ in equation Y = J $\bar{y}$+ $\bar{K}$y.
we can get

$$Y = D\,\bar{Y} + \bar{\bar{D}}$$
$$= D\,\bar{Y} + DY$$

= D ($\bar{y}$ + y)
= D.1 (Because y + y = 1)
= D.

4.3. The T Flip-Flop

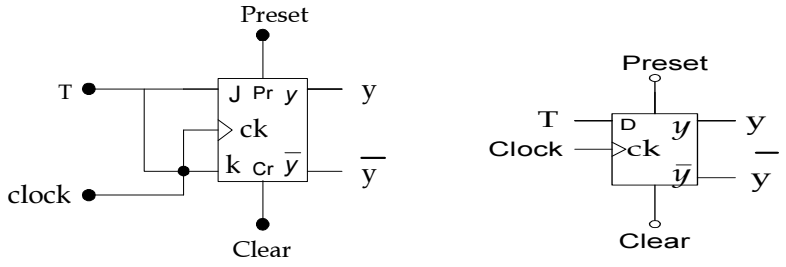
T flip-flop or trigger flip-flop has a single input terminal.

The T flip-flop or trigger flip-flop has a single input terminal. When a clock pulse appears at its input, the state of the T flip-flop is complemented each time irrespective of the present state. Fig. 3.9(b), Fig.3.9(c) and Fig. 3.9(d) represent the symbol, transition table and K-map of the T flip-flop, the characteristic equation of the T flip-flop is given by

$Y = T\bar{y} + \bar{T}y$

The T flip-flop can be obtained from a J-K flip-flop when both the inputs are connected together as shown in Fig. 3.9(a).

The T flip-flop can be obtained from a J-K flip-flop when both the inputs are connected together.



T	y	Y
0	0	0
0	1	1
1	0	1
1	1	0

(c)

] Unchanged
0
] ← Toggle

y \ T	0	1
0	0	0
1	1	1

Y=D (d)

$Y = T\bar{y} + \bar{T}y$
$= T \oplus y$

Fig. 3.9 : T flip-flop; (a) J-K to T conversion, (b) Symbol of T flip-flop, (c) Transition table, (d) K-map.

4.4. Excitation Requirements of Flip-flops

One of the problems in the synthesis of sequential circuits is to find the inputs to the flip-flop for effecting a specified change in its state. All the possible changes in state and the corresponding excitation requirements for various FFs are given in the following excitation requirement table.

Table 3.1: Excitation requirement table.

All the possible changes in state and the corresponding excitation requirements for various FFs.

Present State	Next State	S-R Flip-flop		JK Flip-flop		D flip-flop	T Flip-flop
y	Y	S	R	J	K	D	T
0	0	0	×	0	×	0	0
0	1	1	0	1	×	1	1
1	0	0	1	×	1	0	1
1	1	×	0	×	0	1	0

4.5. T to D Conversion

Let us show the Transition Table for D-FF and T-FF.

D	y	Y
0	0	0
0	1	0
1	0	1
1	1	1

Table : Transition Table for D.

T	y	Y
0	0	0
0	1	1
1	0	1
1	1	0

Table : Transition Table for T.

↓ D	↓ y	Y	↓ T
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

D \ y	0	1
0	0	1
1	1	0

$T = \bar{D}y + D\bar{y}$

$= D \oplus y$

We know that

$D = \bar{T}y + T\bar{y}$

When y=0, Then $D = \bar{T}.0 + T.1 \therefore T = D$

When y=1, then $D = \bar{T} + T.0 = \bar{T} \therefore \bar{T} = \bar{D}$ i.e. $T = \bar{D}$

So, putting $T = D$ we can get

$T = \bar{D}y + D\bar{y}$

$= D \oplus y$

$\therefore T = D \oplus y.$

4.6. D to T Conversion

using truth table

T	y	Y	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	1	0

T \ y	0	1
0	0	1
1	1	0

$D = \bar{T}y + T\bar{y}$

$= T \oplus y$

$\therefore Y = D$

We know that
Y = D
$Y = T \oplus y$
So, $D = T \oplus y$.

4.7. Exercises

4.7.1. Multiple choice questions

a) The T FF is called

i) delay flip-flop
ii) trigger flip-flop
iii) falling flip-flop
iv) none of the above.

b) "Irrespective of the present state it complements when clock pulse occurs". Which one of the following is true for the above statement?

i) T FF
ii) D FF
iii) J-K FF
iv) S-R FF.

4.7.2. Analytical questions

a)
i) How can a JK FF be modified to operate as D F-F?
ii) Construct the characteristics equation of D FF from that of J-K FF?
iii) Why D FF is called Delay FF ?
iv) Explain the operation of D-FF.
v) Draw the Circuit Diagram of D-FF?

b)
i) Why is T -FF called Trigger FF?
ii) Explain T to D and D to T conversion.